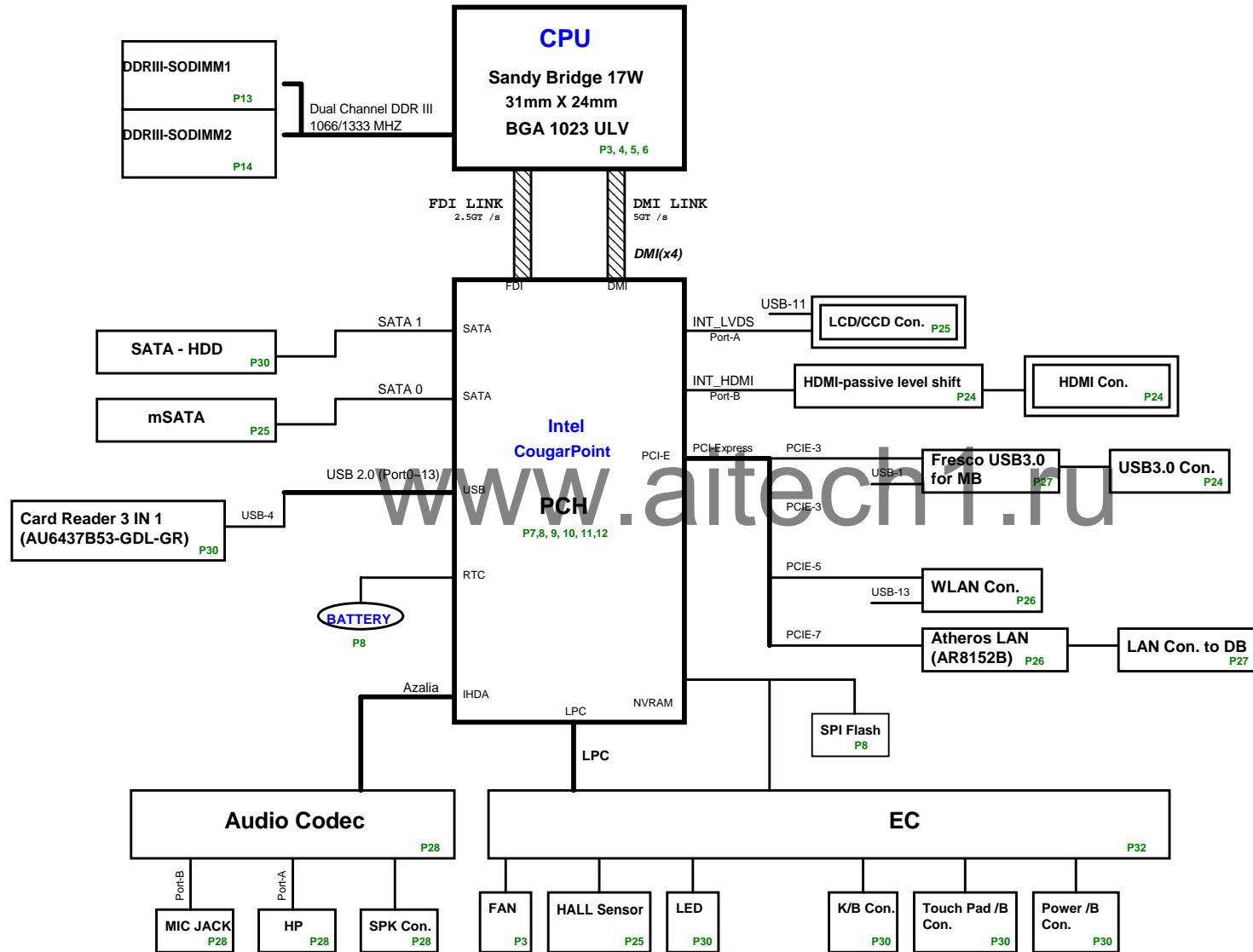


BY1 Block Diagram

PCB HDI Stackups

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SGND
LAYER 5 : SVCC
LAYER 6 : IN2
LAYER 7 : GND
LAYER 8 : BOT



POWER SYSTEM	
ISL88731CHRTZ-T	P33
TPS51123	P34
TPS51216RUKR	P35
OZ80116	P36
TPS51461RGER	P37
ISL95837HRZ-T	P38
G9661-25ADJF12U	P39

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF
+VCCSA

Table of Contents

PAGE	DESCRIPTION	BOI-FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3-6	Processor	CPU
7-12	PCH	CLG
13-14	DDRIII SO-DIMM	DDR
15	S3 Power reduction	
16-23	Blank	Blank
24	HDMI	HDMI
25	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
	LVDS	LCD
	mSATA	SSD
26	Wireless Lan/BT	RF
27	USB 3.0	USB
28	Codec CX20671-21Z	ADO
29	Atheros LAN	LAN
30	INT KeyBoard & K/B LED Power	KBC
	LED Board	LED
	TP connector	TPD
	Power Button	PB
	USB Board/HDD Connector	USB/HDD
31	Cut RTC Battery Power SW	SW
32	EC NPCE795LA0DX	EC
33	Charger (ISL88731C)	PWM
34	System 5V/3V Power	PWM
35	DDR Power	PWM
	+1.05VSUS	LDO
	+1.5V	LDO
36	+1.05V/VT	PWM
37	+VCCAS	PWM
38	+VCC_Core	PWM
39	+1.8V	LDO
	Discharge(3V/5V/+1.5V)	LDO
40	EE Change List	

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
AGND_DC/DC	34
ADOGND	All
GND	28

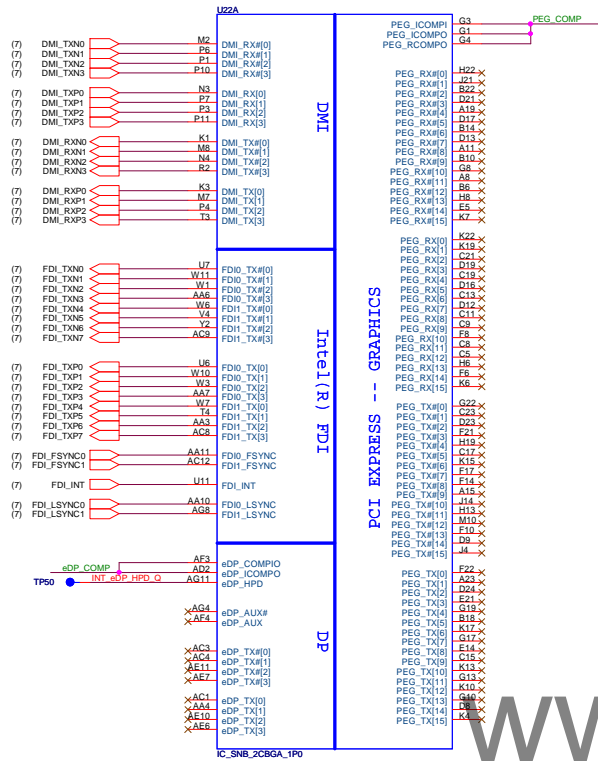
ITEM	Value Code	FUNCTIONS
1	IVB@	Ivy Bridge
2	SNB@	Sandy Bridge
3	IV@	UMA
4	U3@	USB 3.0
5	IU3@	USB 2.0 and Chief River (colay W USB 3.0)
6	HM@	HDMI
7	IHM@	Internal HDMI
8	C@	Cost issue



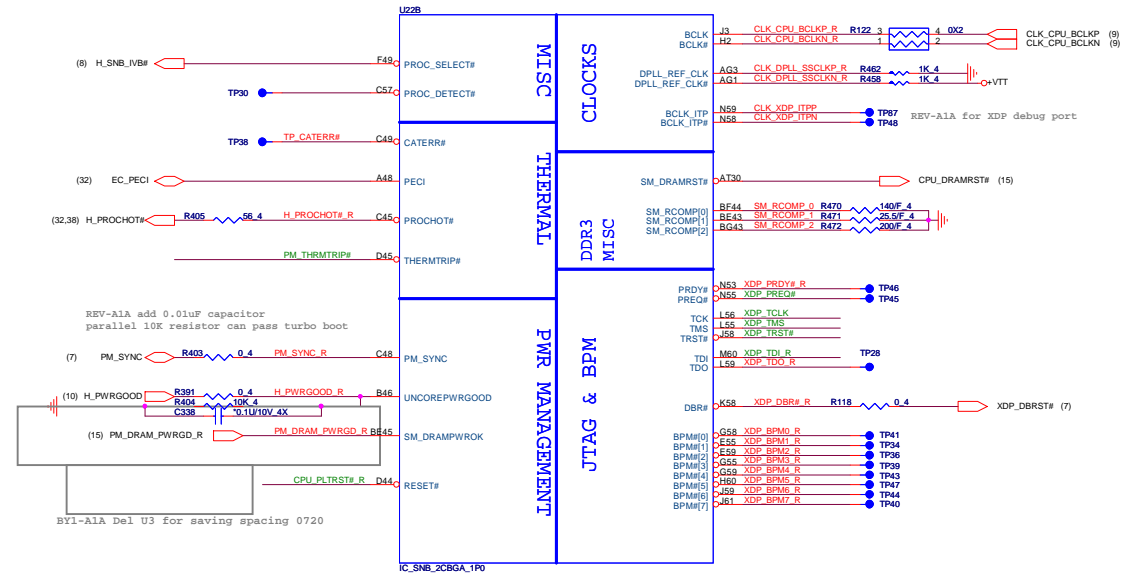
Quanta Computer Inc.

PROJECT : BY1

Sandy Bridge Processor (DMI,PEG,FDI)



Sandy Bridge Processor (CLK,MISC,JTAG)



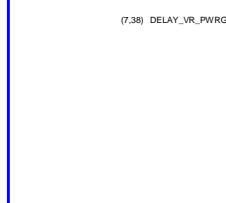
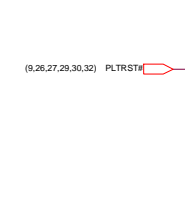
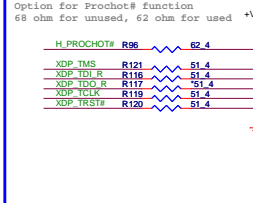
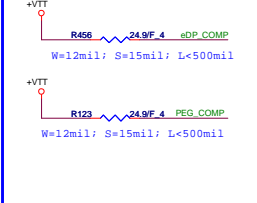
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FDI Disabling (Discrete Only)
<CPU>DP & PEG Compensation
<CPU>

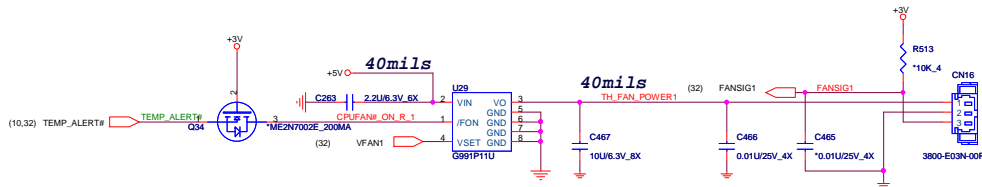
Processor pull-up <CPU>

Level Shift <CPU>

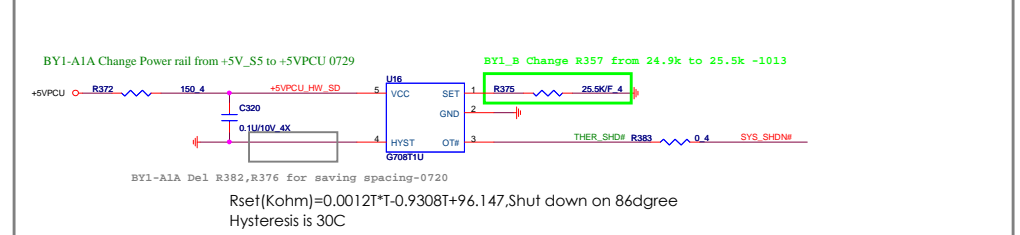
Thermal Trip <CPU>



FAN Control-->For one FAN solution <THC>



CPU Thermal sensor / MB Local TEMP <THC>

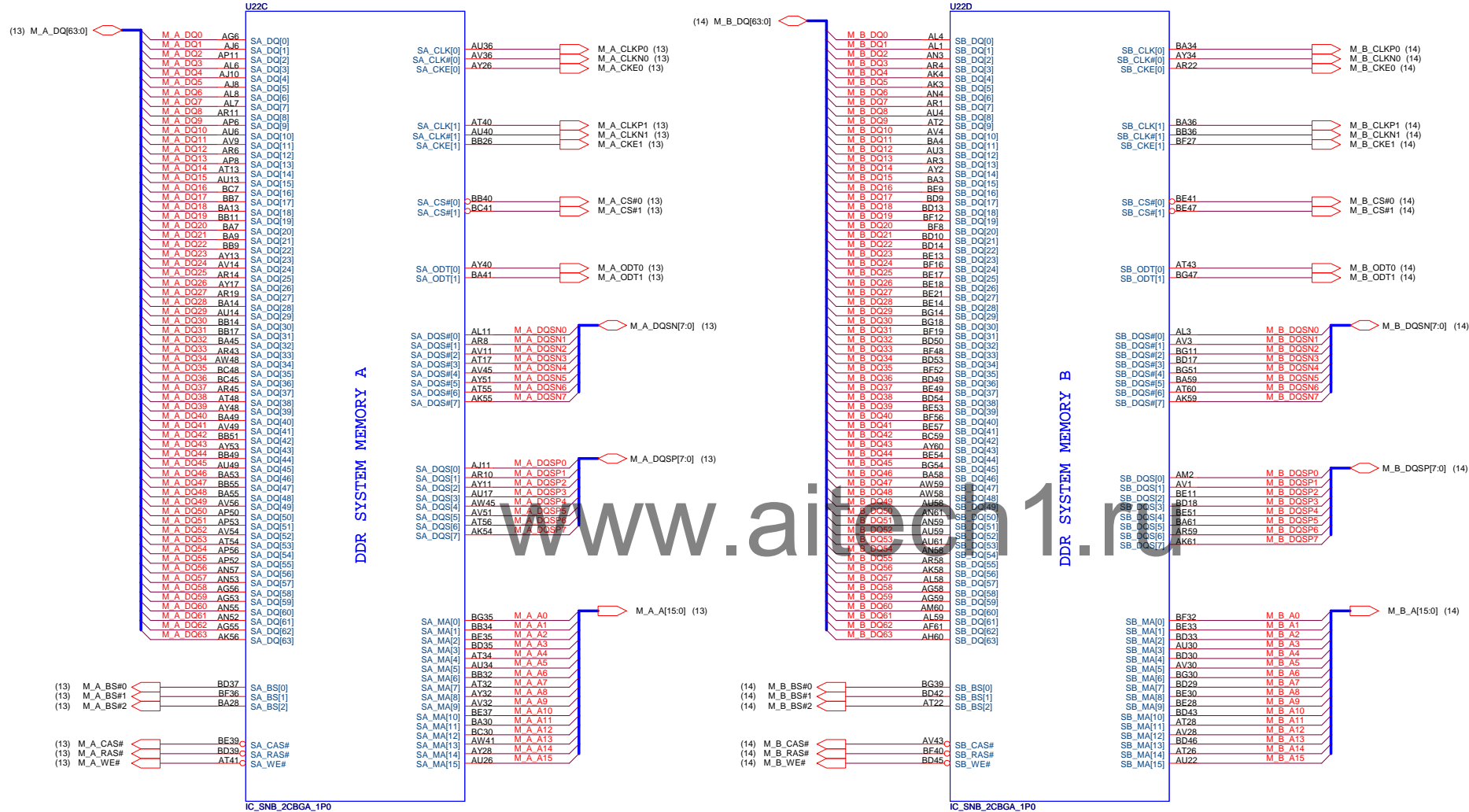


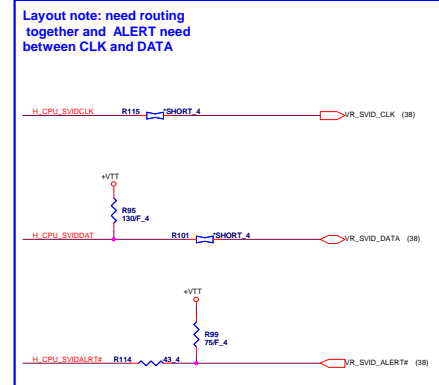
REV-C3A Change VCC PINS of U3 from +3VPCU to VL
Add R496,R497,R499
Reverse R14,R498,R31,R24,Q3

Sandy Bridge Processor (DDR3)

04

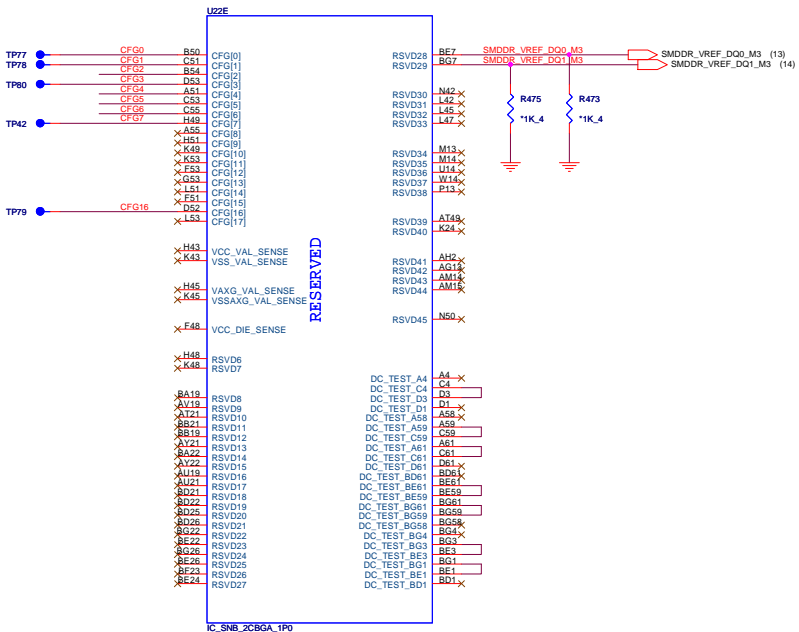
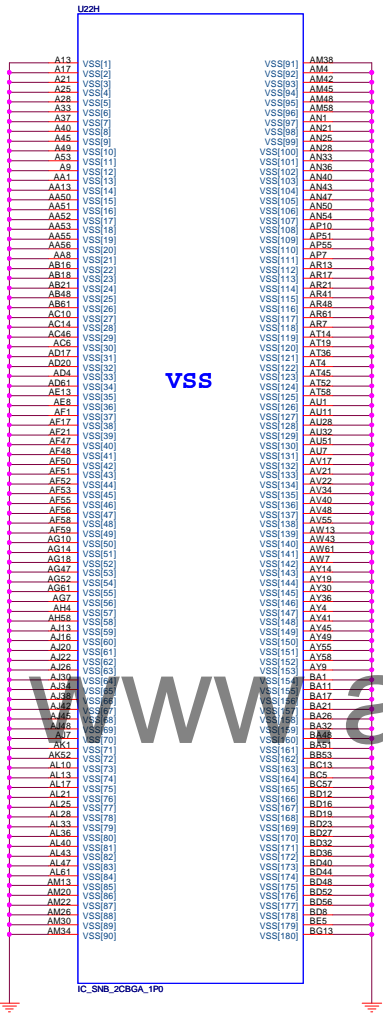
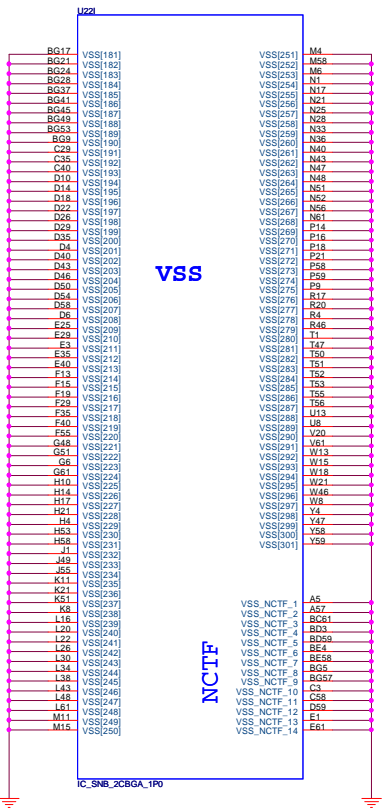
BY1-A1A Add B Channel Memory
0826 Jerry





Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)

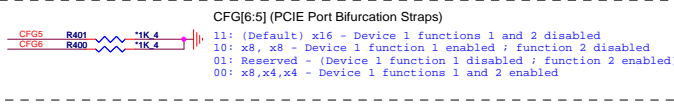
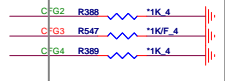


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Processor Strapping

The CFG signals have a default value of "1" if not terminated on the board.

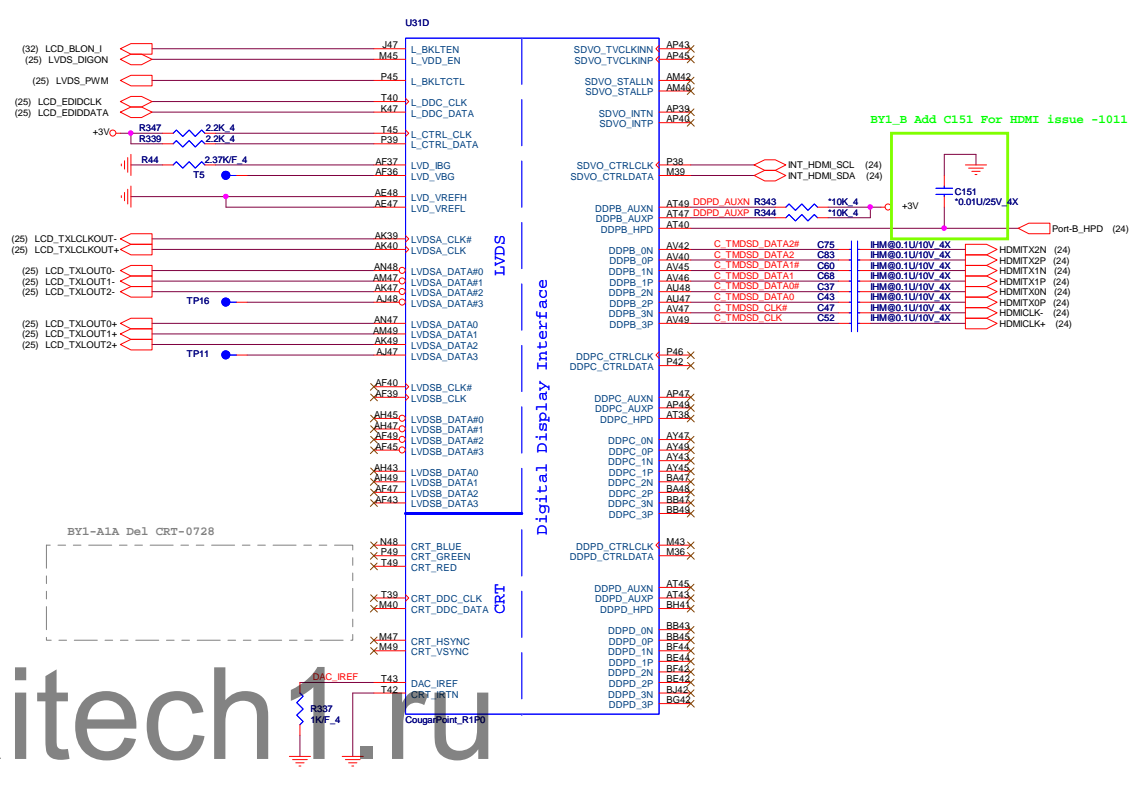
CFG2	1	0
(PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3	Normal Operation	Lane Reversed
(PCI-E Static x4 Lane Reversal)		
CFG4	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
(DP Presence Strap)		



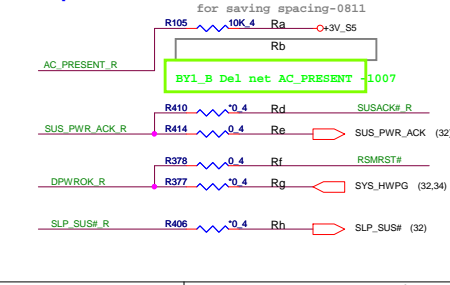
CFG[6:5] (PCIe Port Bifurcation Straps)

- 11: (Default) x16 - Device 1 functions 1 and 2 disabled
- 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
- 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
- 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Cougar Point (LVDS,DDI)

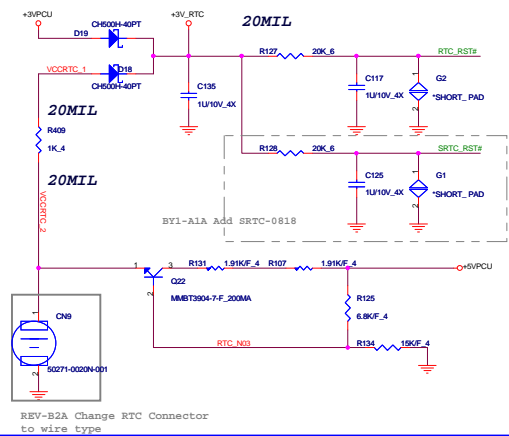


Deep Sx <CLG>

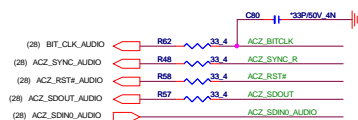


Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

RTC Circuit <RTC>



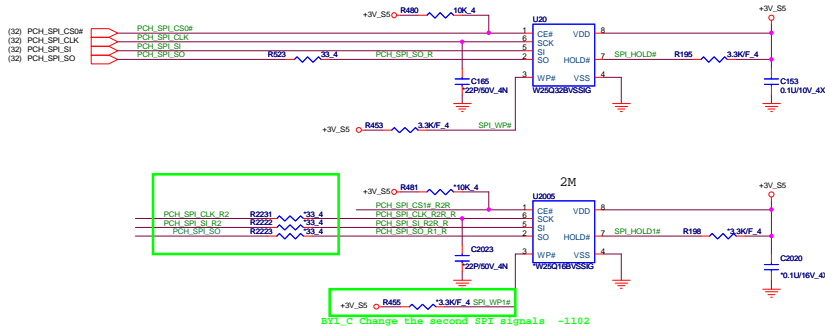
HDA Bus <ADO>



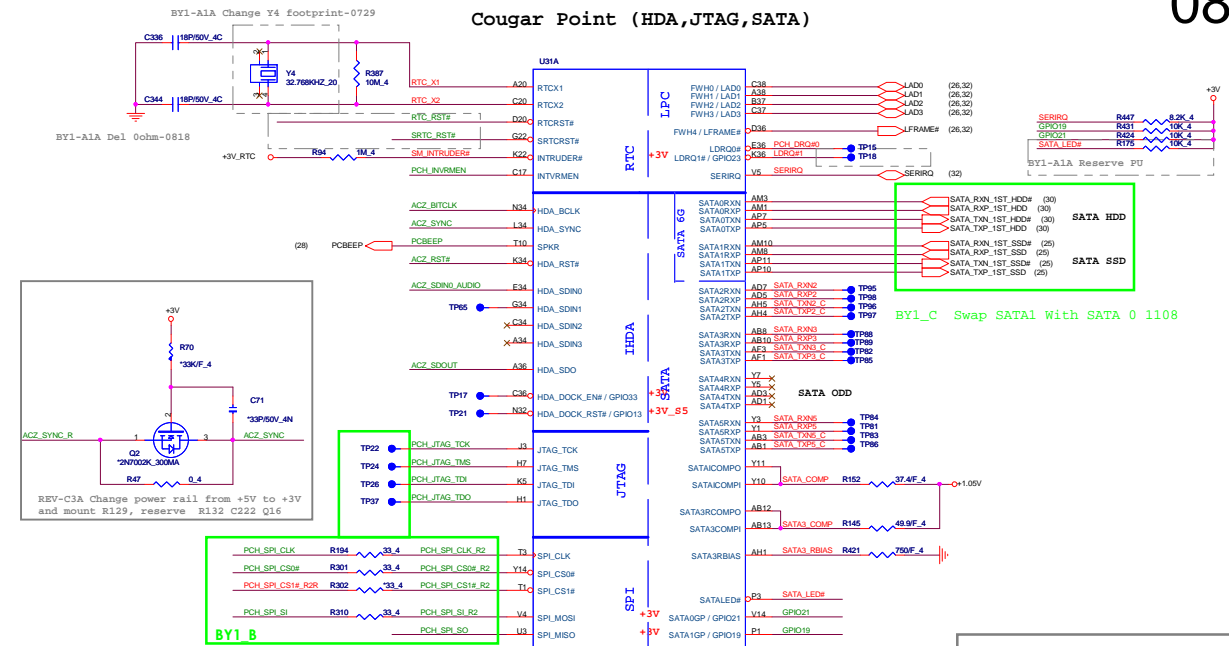
PCH JTAG Debug (CLG)

BY1_B Del for saving spacing-1007

PCH Dual SPI (CLG)

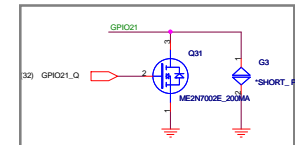
 MX25L3205DM2I-12G; AKR39FP0Z00
 W25X32V8S1G; AKR39ZP0N00


PCH2 <CLG> <ADO> <RTC>



PCH Strap Table

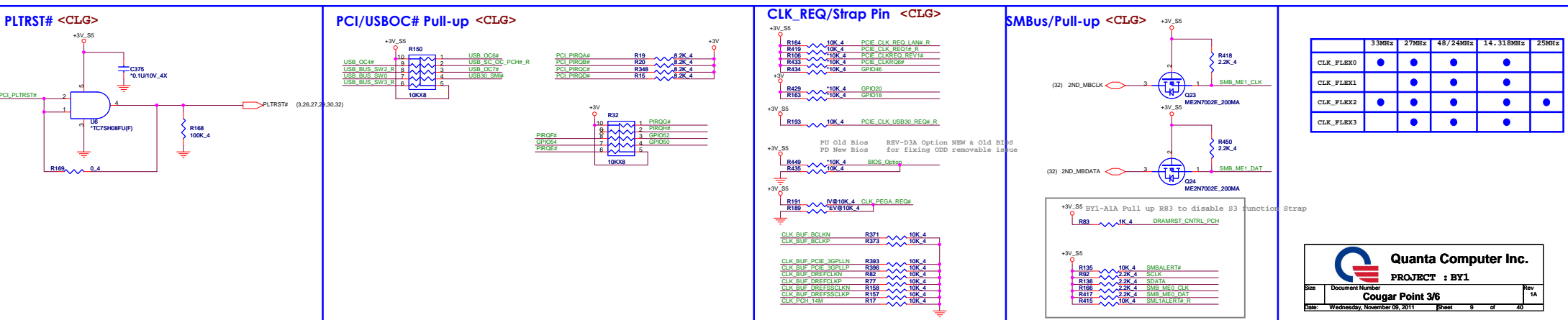
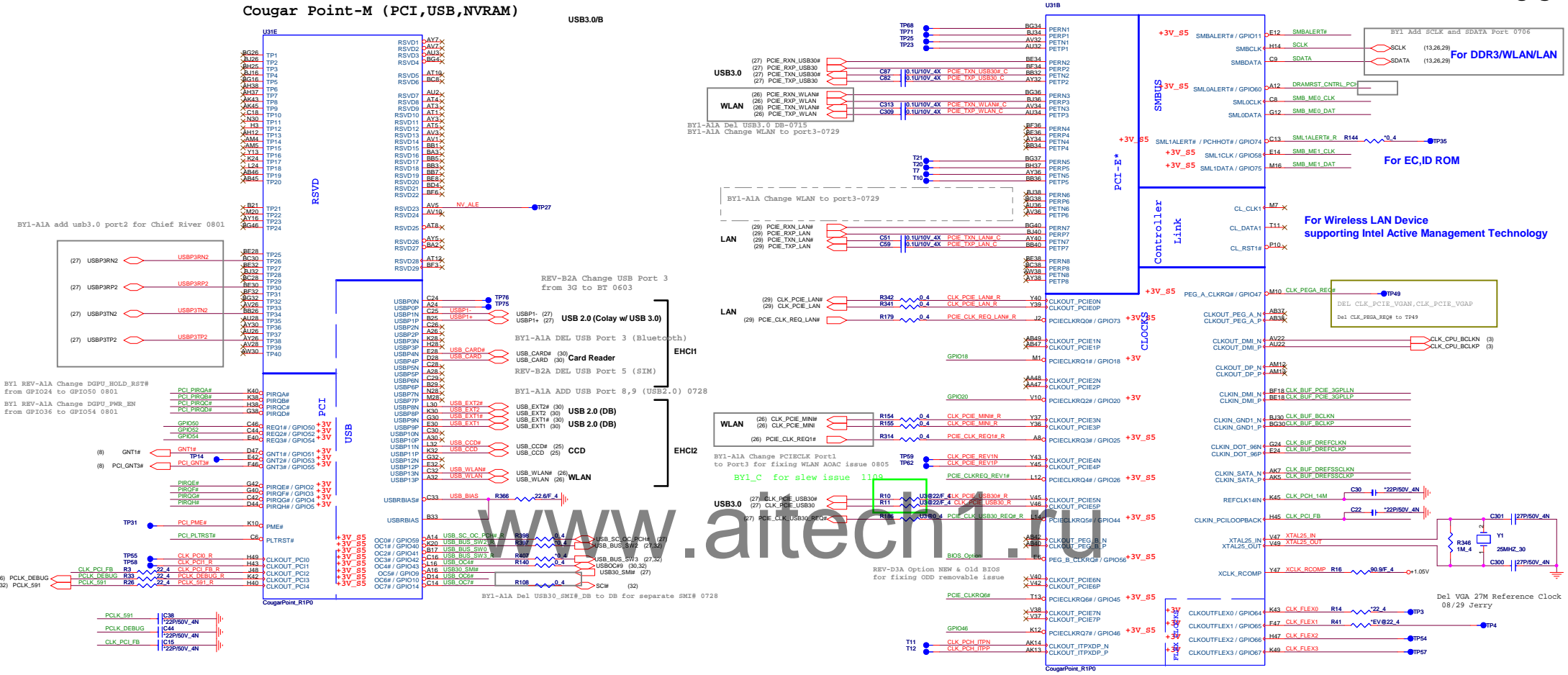
Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V_PCU R432 *1K_4 PCBEEP									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R362 *1K_4 PCH_GNT3# (9)									
INTVRMEN	Integrated 1.05V/VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R84 *330K_4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GPIO19</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	GNT1#	GPIO19	Boot Location	1	1	SPI *	0	0	LPC	R49 *1K_4 GNT1# (9) R441 *1K_4 GPIO19
GNT1#	GPIO19	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_PCU R55 *1K_4 ACZ_SDOOUT (32)									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R423 *2.2K_4 DF_TVS (10) R427 *1K_4 H_SDO_IN (3)									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3V_PCU R443 *10K_4 PLL_OVR_EN (10)									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R50 *1K_4 ACZ_SYNC									
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 R132 *1K_4 GPIO15 (10)									
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	+3V_RTC R89 *330K_4 DSWVRMEN (7)									
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect									
GNT2# / GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile									
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
SATA3GP / GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
SATA2GP / GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									


 REV-B2A Add G3 for Clear CMOS password
 BU7-A1A Modify Clear CMOS password
 control by EC GPIO77-0720
 BY1-A1A Add G3 for Clear CMOS password-0728

Cougar Point-M (PCI,USB,NVRAM)

USB3.0/B

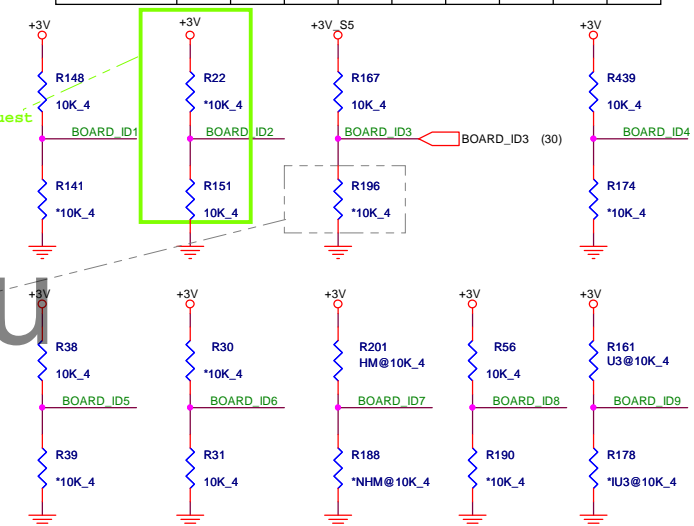
<CLG> <U3B> <USB> <MNW> <MNT> <LAN>



	33MHz	27MHz	18/24MHz	14.318MHz	25MHz
CLK_FLEX0					
CLK_FLEX1					
CLK_FLEX2					
CLK_FLEX3					

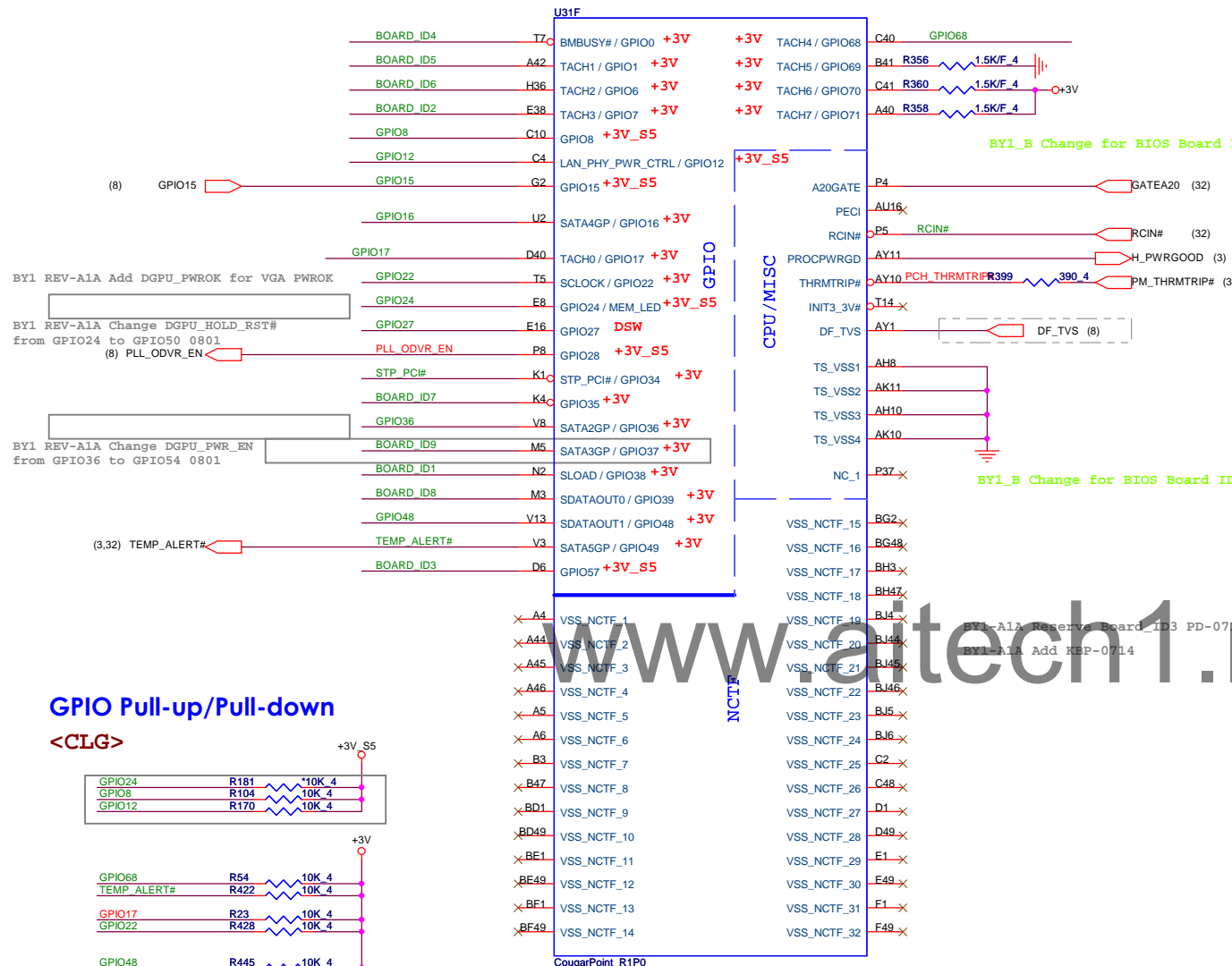
BOARD ID SETTING <CLG>

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
BU6 SKU KZ1 SKU	H L								
BY1D BY1		H L							
W/O LED KB W/ LED KB			H L						
Reserve				H L					
Reserve					H L				
W/O CCD W/ CCD						H L			
W/ HDMI W/O HDMI							H L		
BY1 BU6 or KZ1								H L	
W/ USB3.0 W/O USB3.0									H L

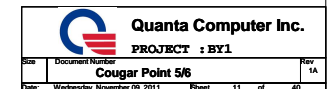


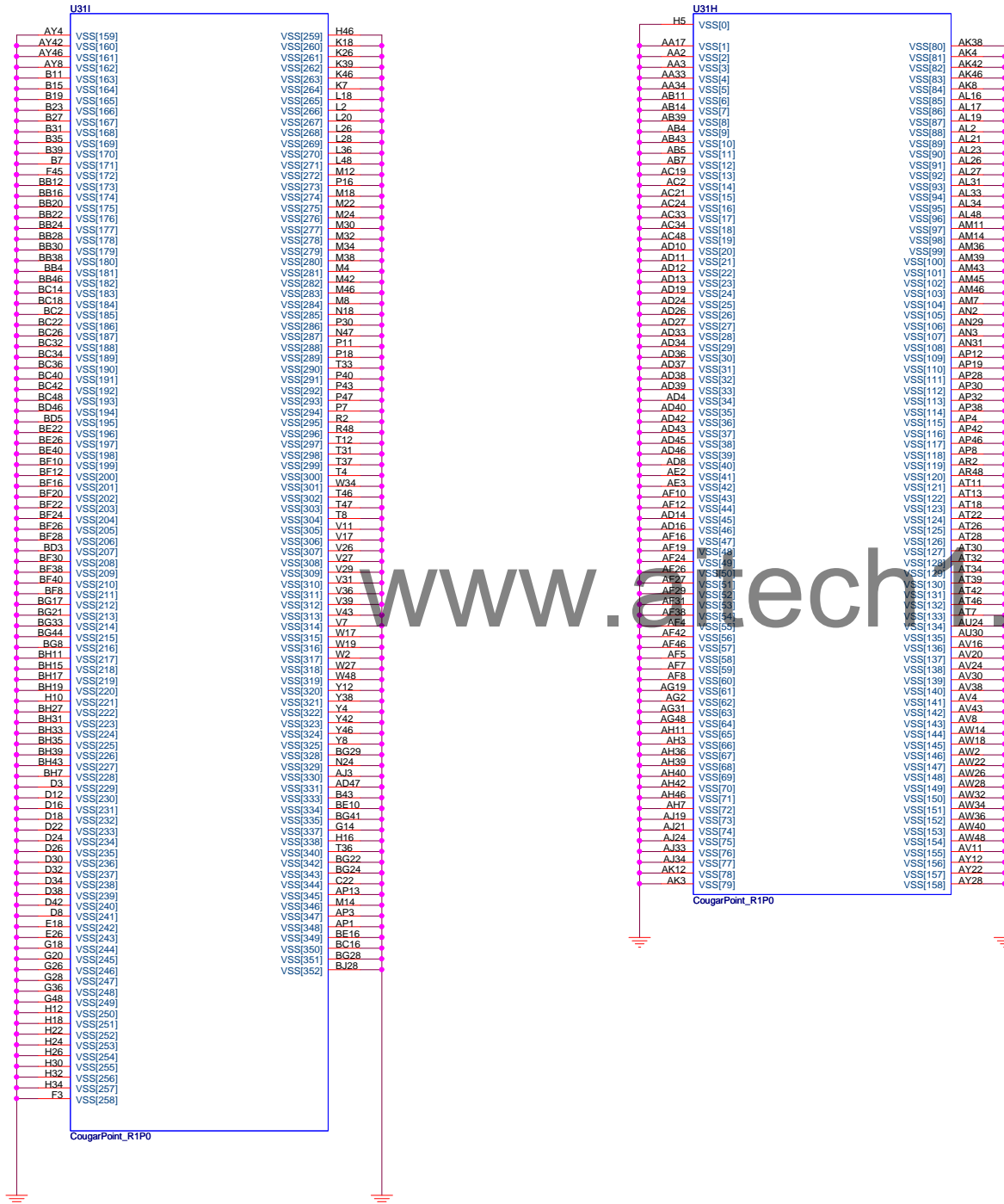
BY1-A1A Del RAM Configuration Table-0811

Cougar Point (GPIO,VSS_NCTF,RSVD)



Cougar Point-M (POWER)

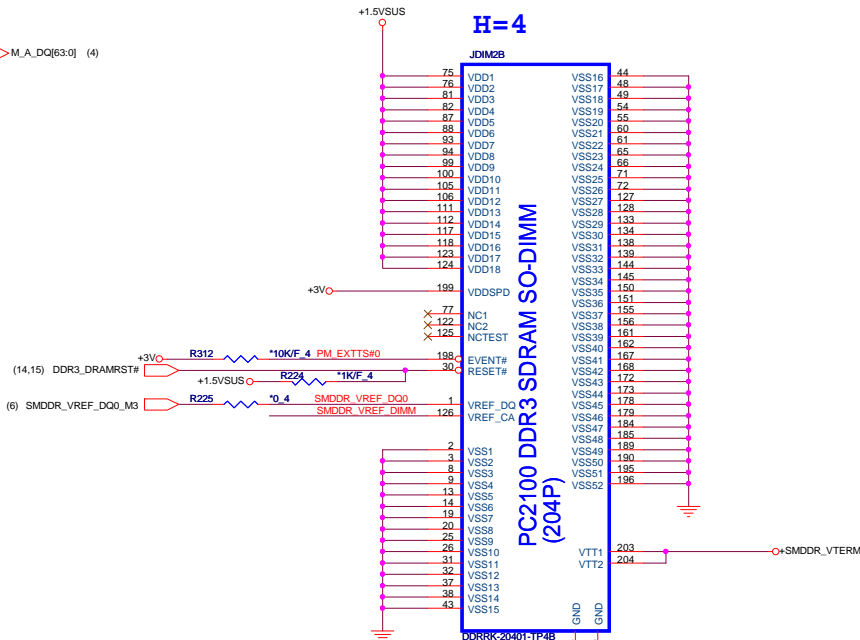




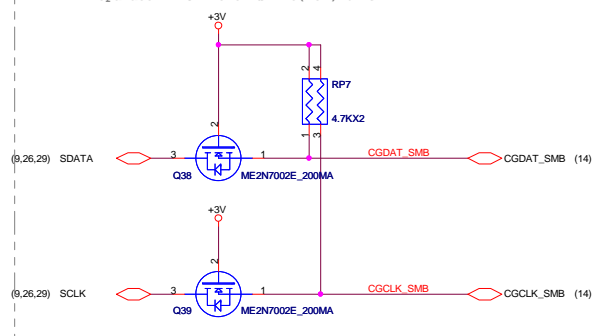
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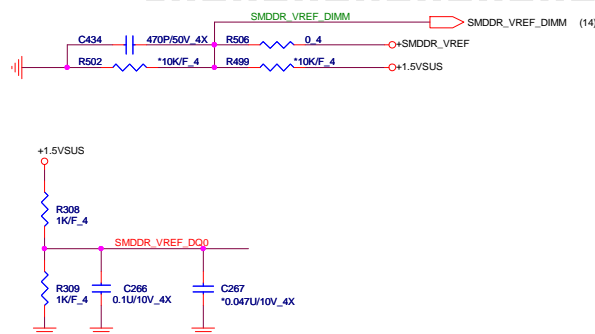
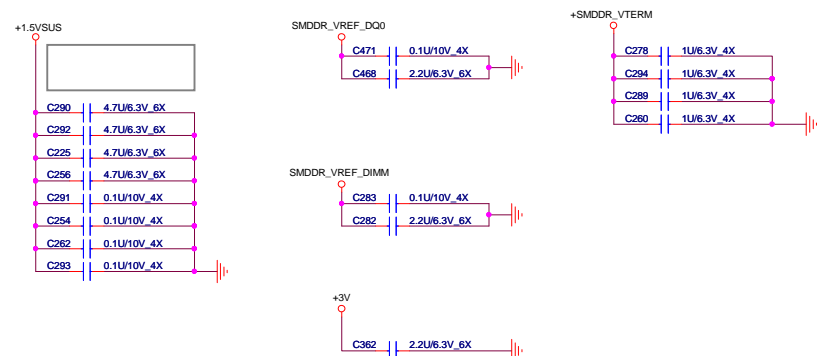
Size	Document Number	Rev
	Cougar Point 6/6	1A
Date:	Wednesday, November 09, 2011	Sheet 12 of 40



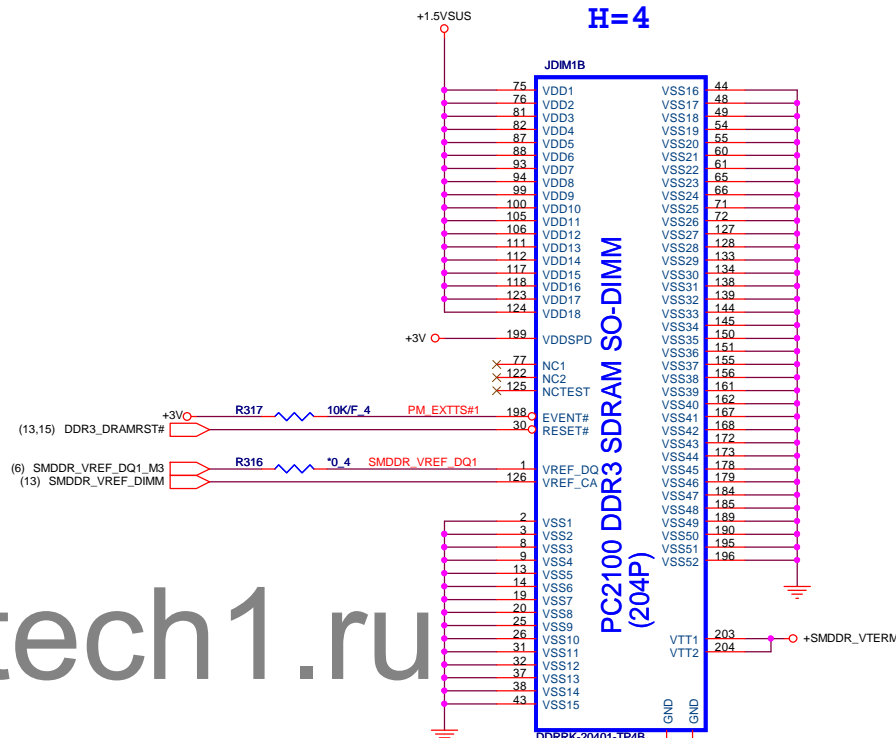
SMBus(DDR3/WLAN/LAN)
BY1-A1A Separate SMBUS level shift(+3V)-0729



BY1 Del C218 and C255 for saving space 0720



H=4



+1.5V_SUS

Capacitor	Value	Voltage Rating	ESR
C45	4.7uF	6.3V	6X
C114	4.7uF	6.3V	6X
C107	4.7uF	6.3V	6X
C48	4.7uF	6.3V	6X
C105	4.7uF	6.3V	6X
C104	4.7uF	6.3V	6X
C62	0.1uF	10V	4X
C74	0.1uF	10V	4X
C137	0.1uF	10V	4X
C138	0.1uF	10V	4X

SMDDR_VREF_DIMM

Capacitor	Value	Voltage Rating	ESR
C139	0.1uF	10V	4X
C145	2.2uF	6.3V	6X

+SMDDR_VTERM

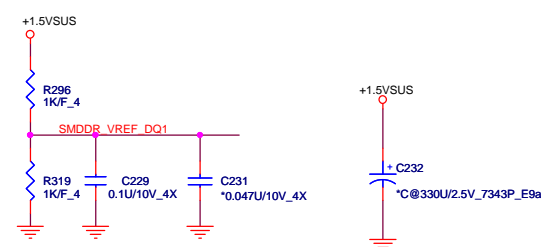
Capacitor	Value	Voltage Rating	ESR
C228	1uF	6.3V	4X
C215	1uF	6.3V	4X
C223	1uF	6.3V	4X
C226	1uF	6.3V	4X

SMDDR_VREF_DQ1

Capacitor	Value	Voltage Rating	ESR
C147	0.1uF	10V	4X
C218	2.2uF	6.3V	6X

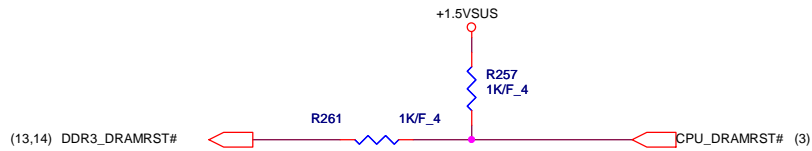
+3V

Capacitor	Value	Voltage Rating	ESR
C221	2.2uF	6.3V	6X



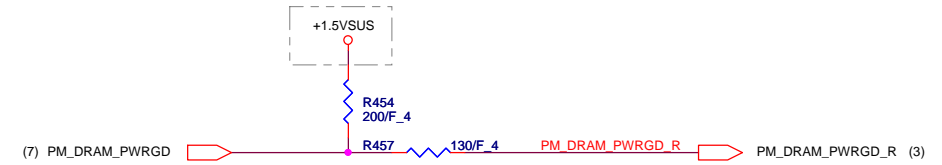
S3 power Reduction (SM_DRAMRST#) <S3P> <4>

BY1-A1A Del S3 power reduction-0714



S3 power Reduction (SM_DRAMPWROK) <S3P> <3> 15

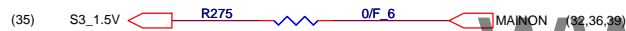
BY1-A1A Del S3 power reduction-0714



R454 external pull-up resistor
close to the processor.
A series-resistor of R457 is required between
the pull-up resistor and the processor

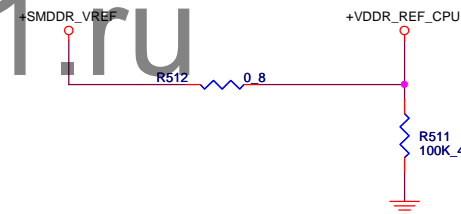
For S3 power Reduction Sequence <S3P> <3>

BY1-A1A Del S3 power reduction-0714



S3 power Reduction (CPU Power) <S3P> <5>

BY1-A1A Del S3 power reduction and change +1.5V_CPU to +1.5VSUS 0714



For S3 power Reduction VTT discharge <S3P> <13>

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PROJECT : BY1

Size	Document Number	Rev
	ROBSON_XT_PCIE_Interface	1A

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Size	Document Number	Rev
	RS/SM-S3_Power_and_NC	1A
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	ROBSON/MEM_Interface	1A
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Size	Document Number	Rev
	Seymour S3 VRAM(DDR3 BGA96)	1A
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PROJECT : BY1

Size

Document Number

BACO

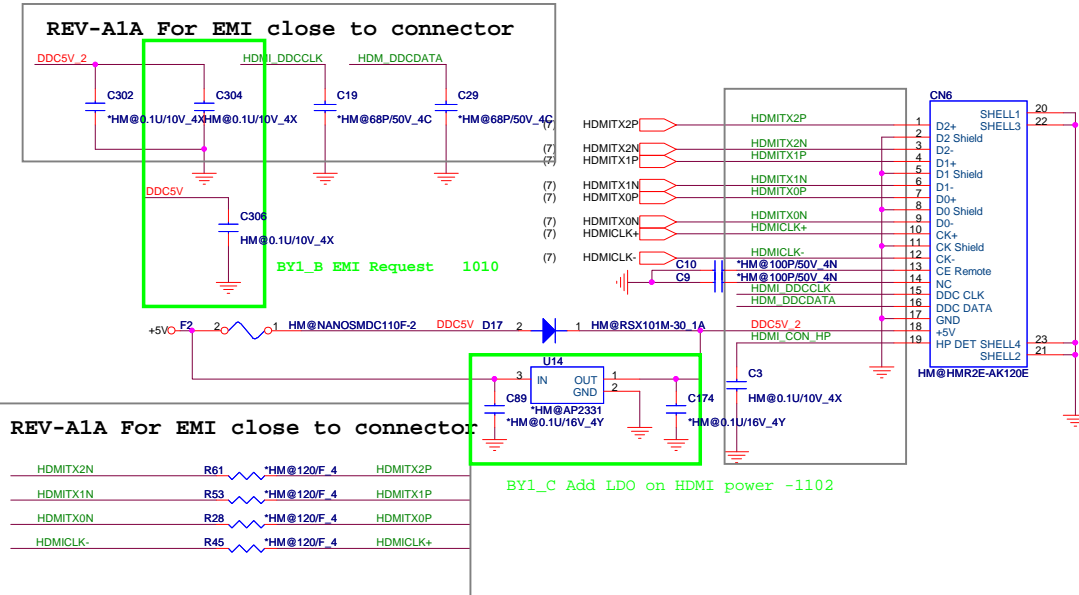
Rev

1A

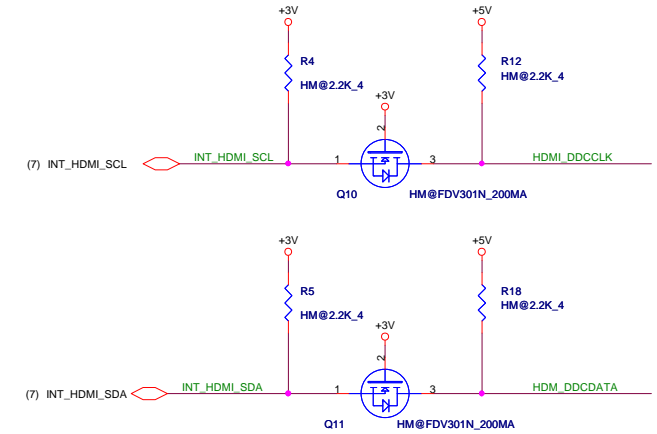
Date: Wednesday, November 09, 2011

Sheet 23 of 40

HDMI Conn <HDM>

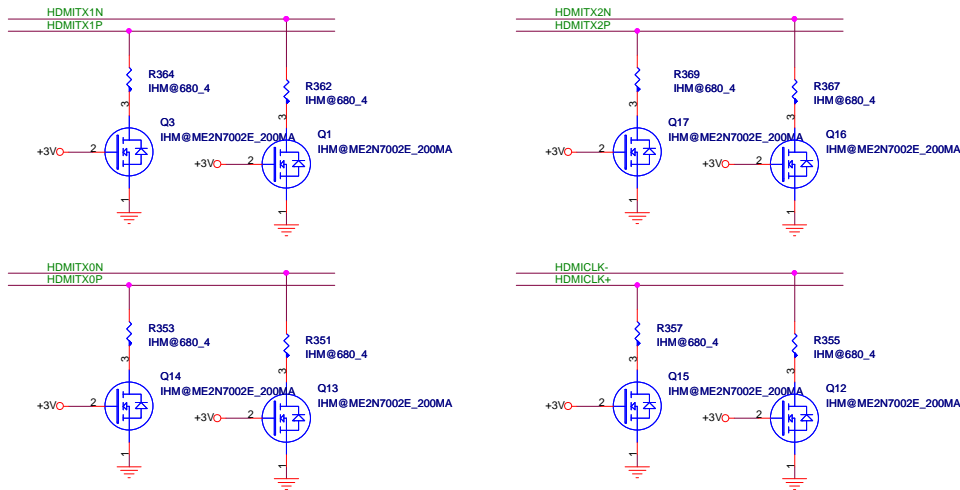


HDMI-SMBus <HDM>

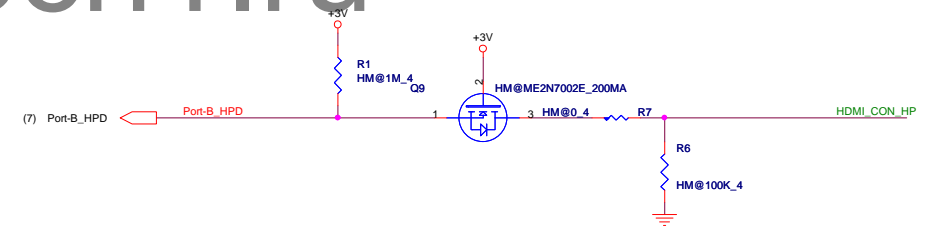


16

HDMI-passive level shift <HDM>

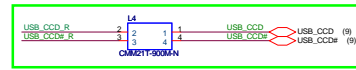


HDMI-HPD <HDM>



CCD <CCD>

BY1_C Change L4 footprint to choke-diplms900h12l-4p-1 -1102



0.2A(20mils)

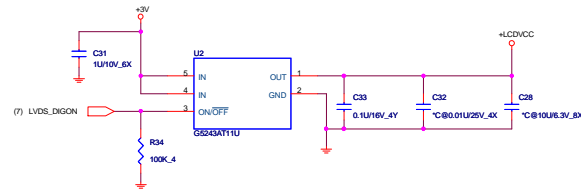
BY1-A1A Del 1000p-0817

BY1_B Unmount C23 1007

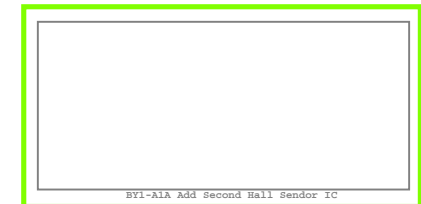
BY1_B Del F1 1007

LCD POWER SWITCH <LDS>

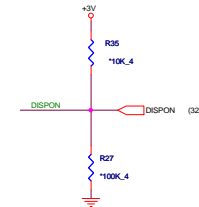
BY1-A1A Change U2 footprint from 6 pin to 5 pin and change 2nd source-0812



HALL SENSOR&BACK LIGHT SWITCH <HSR>

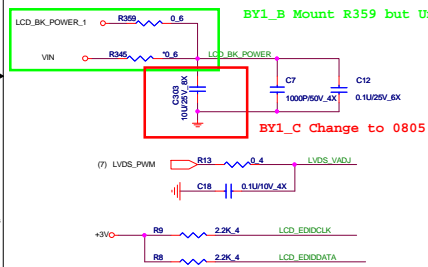


BY1_B Del second hall sensor HX1,R300,C335 for save space -1006

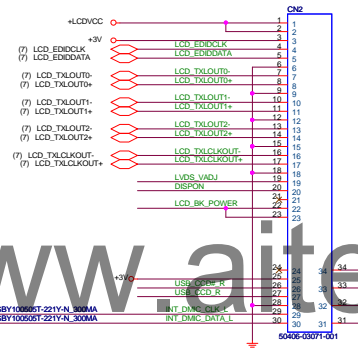


LCD Panel Module <LDS>

BY1_B Mount R359 but Unmount R345



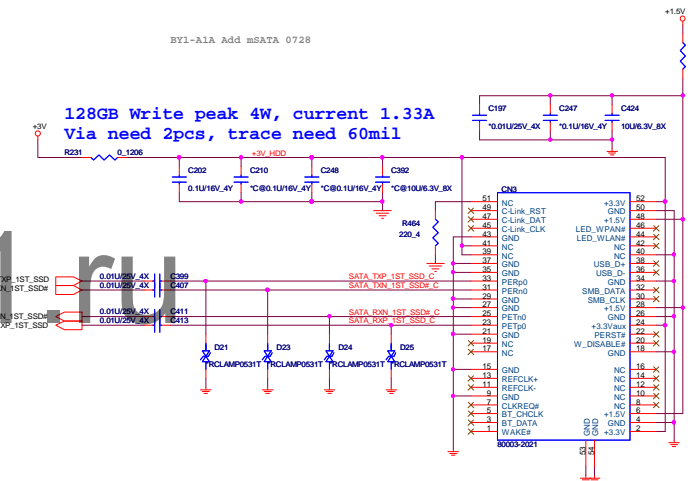
BY1_C Change to 0805



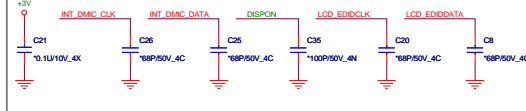
mSATA (SATA over mini PCIe)

<H1D>

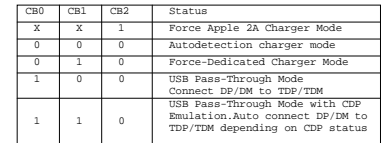
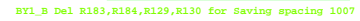
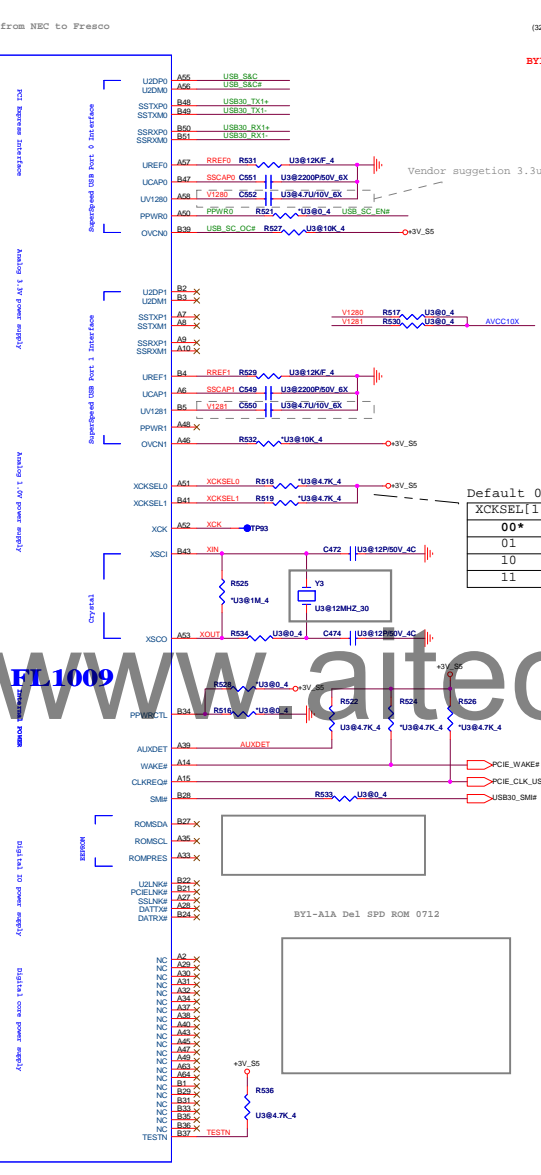
BY1-A1A Add mSATA 0728

128GB Write peak 4W, current 1.33A
Via need 2pcs, trace need 60mil

REV-A1A For EMI close to connector

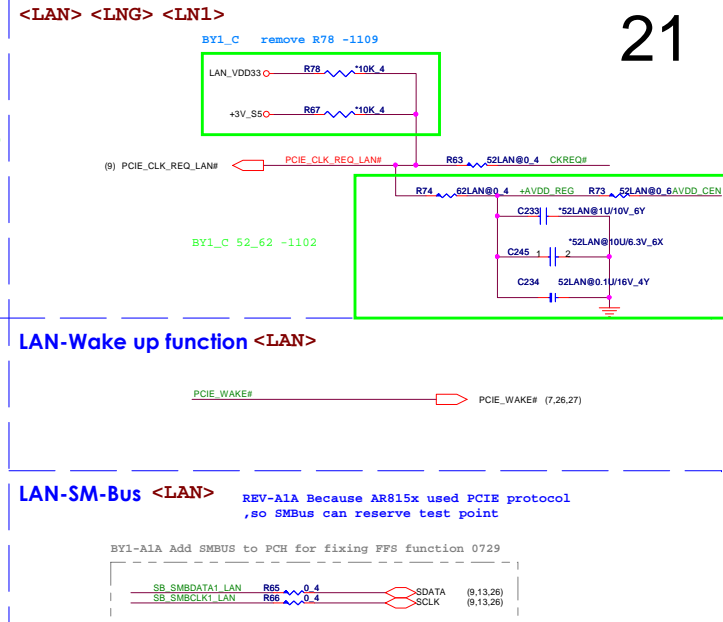
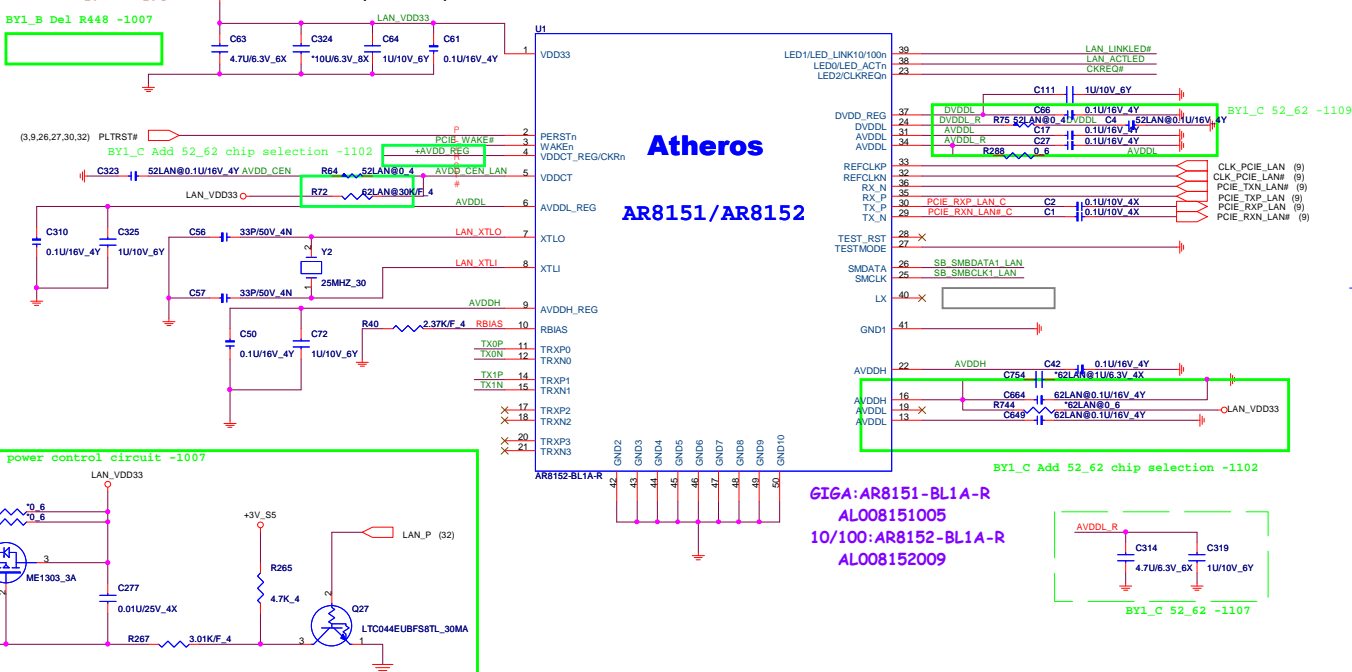


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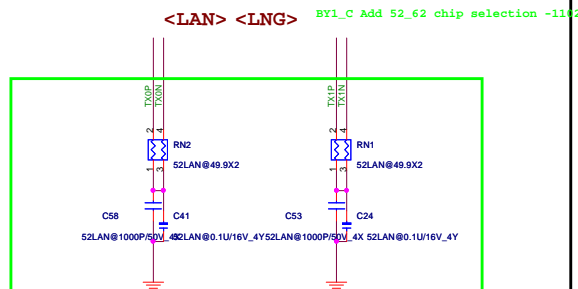


[illegible][illegible][illegible]

Atheros Lan <LAN> <LNG> LAN_VDD33 0.163A(20mils)



PLACE NEAR LAN IC SIDE



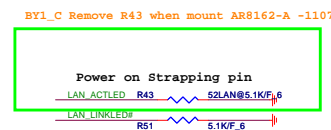
A<LAN> <LNG>

SIGNALS

CONNECTOR

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R <LAN> <LNG> <LN1>



LEDO = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode



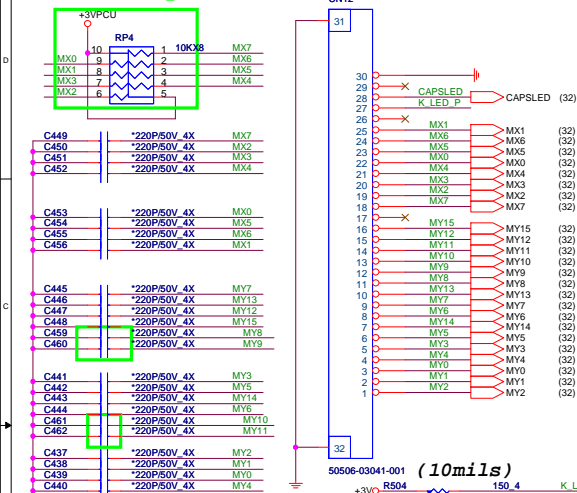
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Size	Document Number	Rev
	Atheros LAN (AR8151B/52B)	1A
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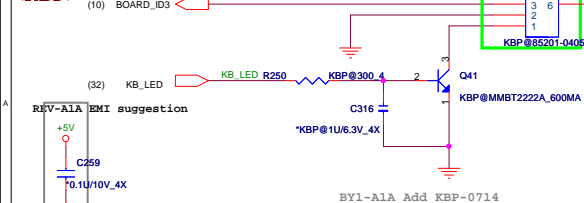
INT KeyBoard <KBC> <EMI>

BU7-A1A Change to 30pin connector
BY1-A1A NC-0817BY1_C Add PU 10k for KB CN16... -1102



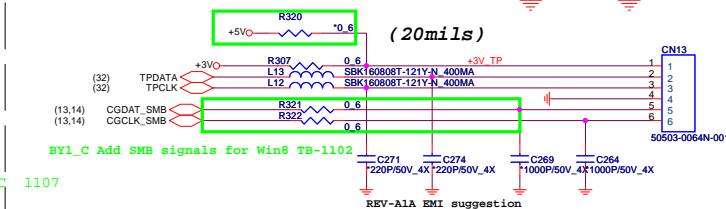
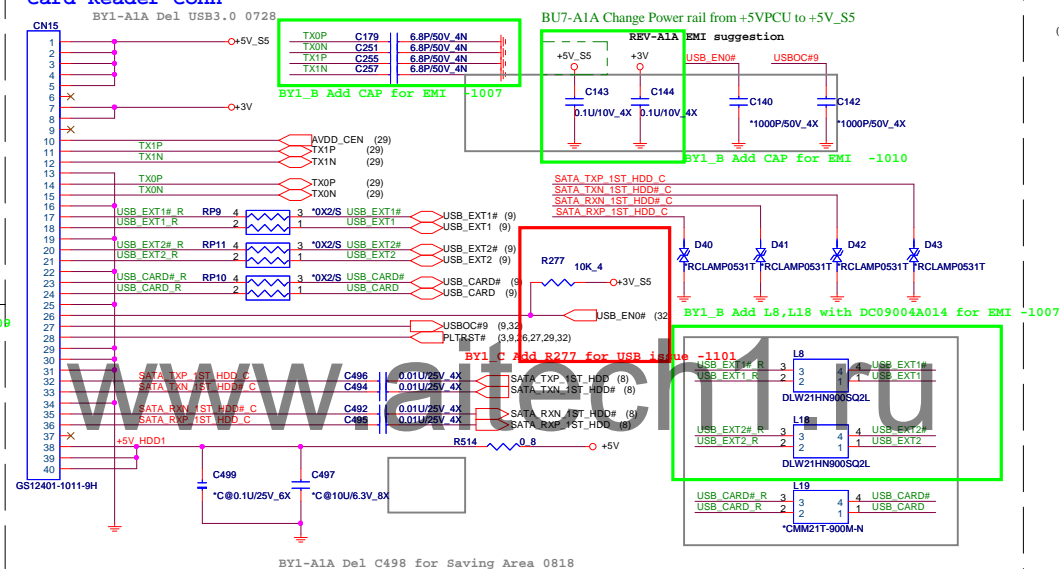
K/B LED power

<KBP>

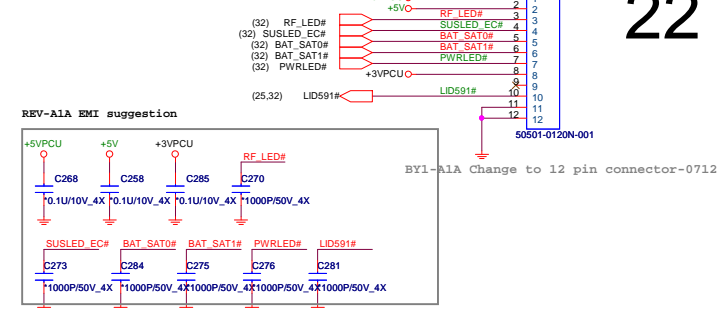


TP board <TPD> <EMI>

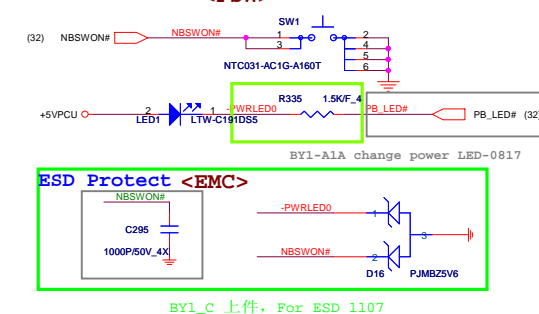
BY1_C Add +5V for Win8 TB-1102

LAN&USB&Cardreader & HDD Interface <U3B> <MMC> <EMI> <H1D> <LAN>
Card Reader Conn

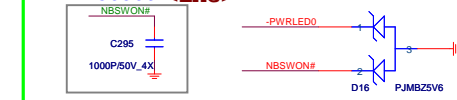
LED <LED>



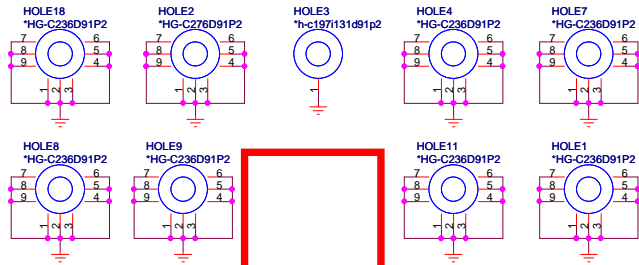
Power Button <PSW> BY1_B Change R335 from 150 to 1.5k



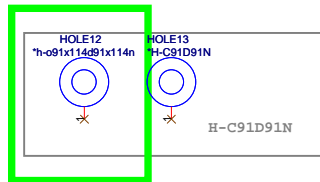
ESD Protect <EMC>



HOLE <OTH>

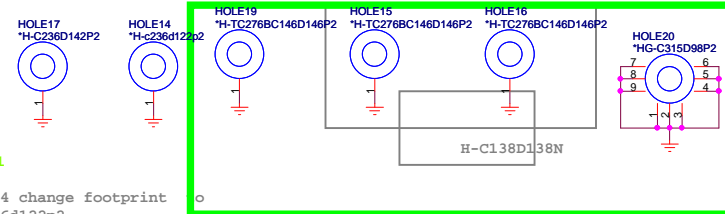


BY1_B Change HOLE1,HOLE4,HOLE7,HOLE8,HOLE9,HOLE10,HOLE11,HOLE18 Footprint 1011



BY1_B HOLE 12 change footprint to h-o91x114d91x114n

BY1_B HOLE 20 Footprint 1012



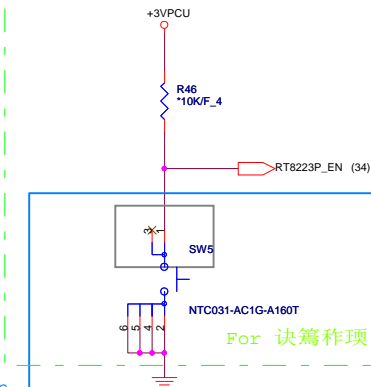
BY1_B HOLE 14,HOLE 15,HOLE19,HOLE16 to ground for EMI 1007

hole 14 change footprint to
h-c236d122p2
Jerry 0902

hole 17 footprint change to H-C236D142P2
Jerry 0902

BU7-A1A Add cut battery power circuit-0725
BU7-A1A Del cut battery power circuit from HW solution, change to only control from ME solution-0727

BU7-A1A Modify cut battery power circuit-0729



BY1-A1A Modify SW5 PIN 3 to NC for fixing Layout issue 0819

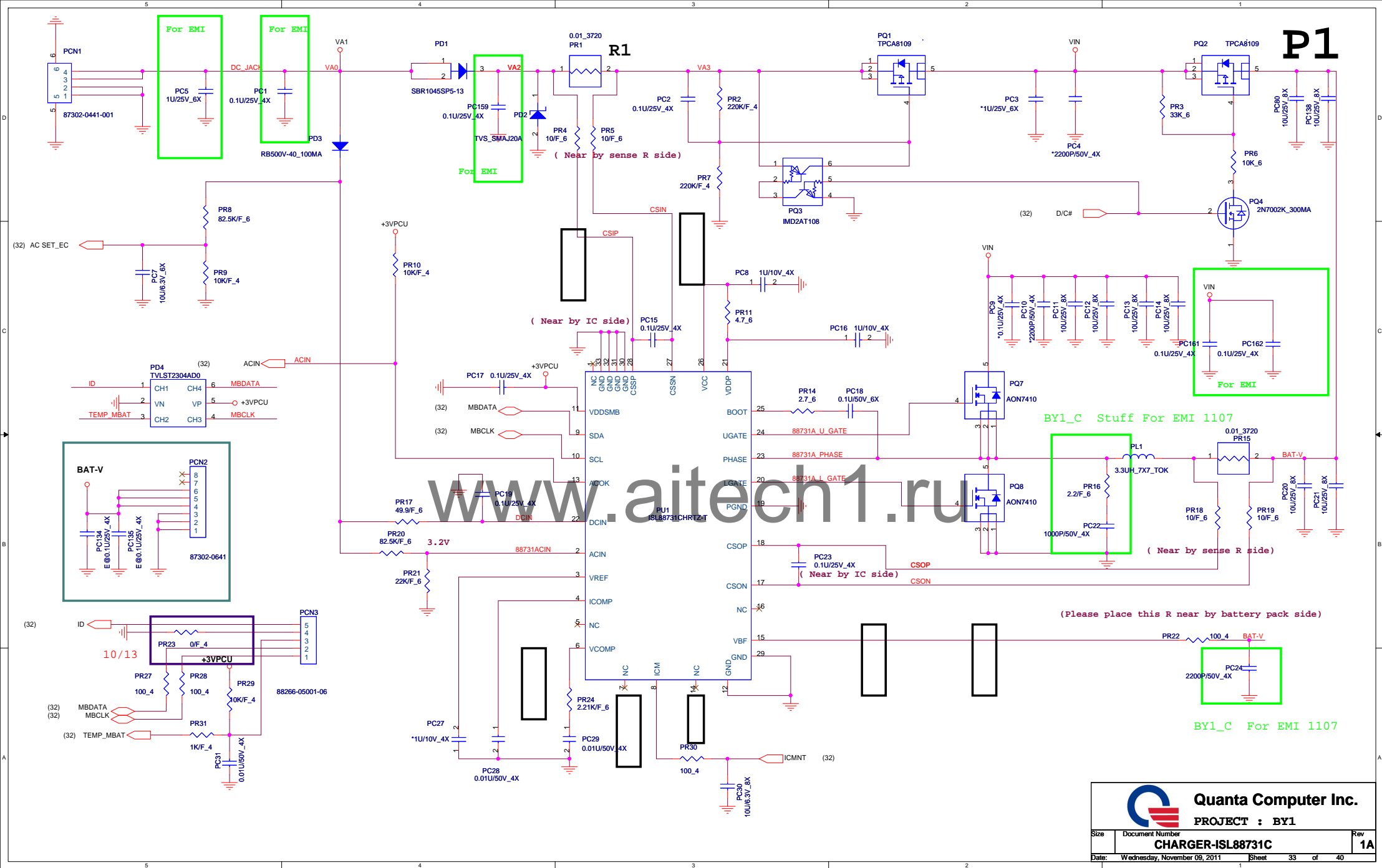
For EE&SW solution

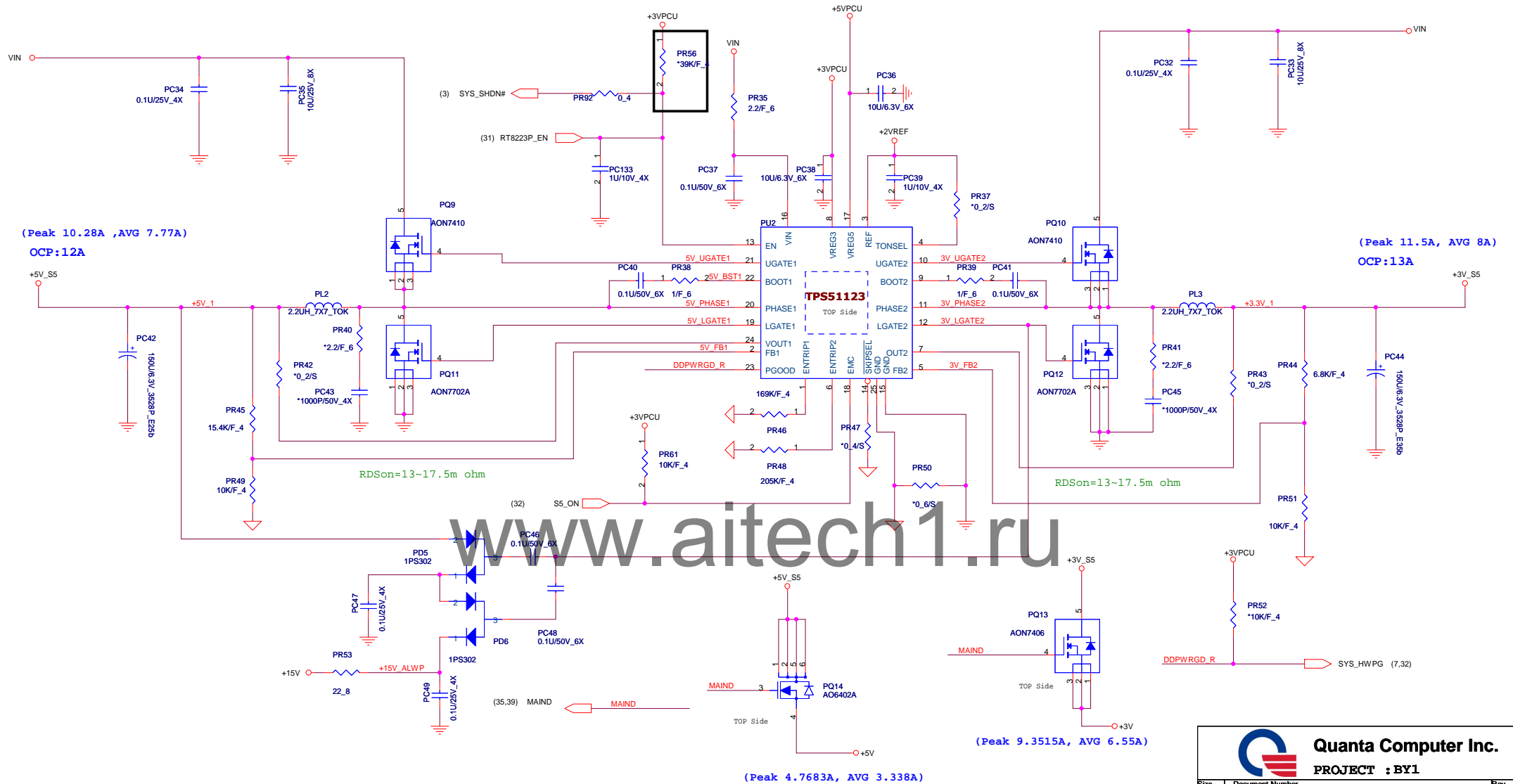


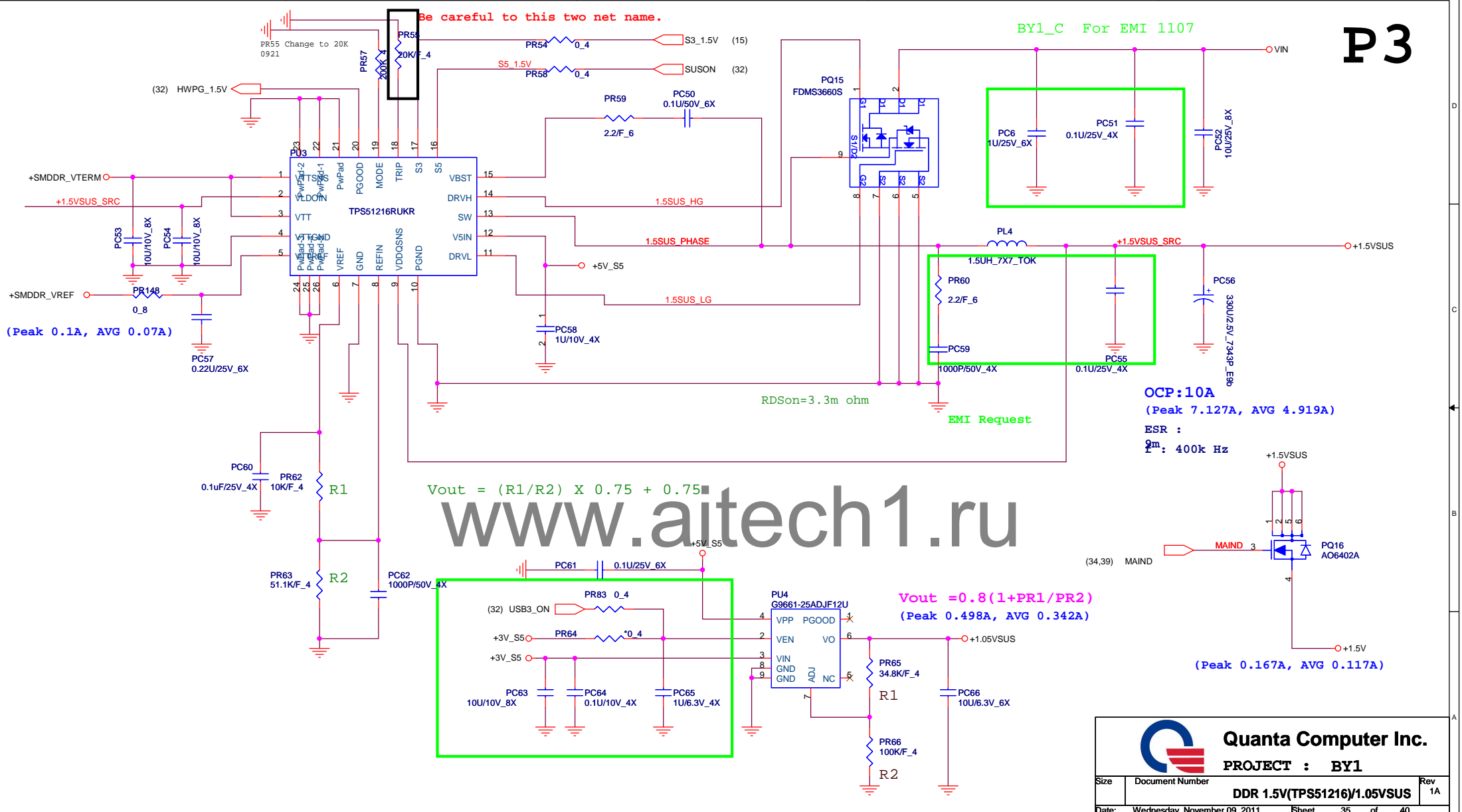
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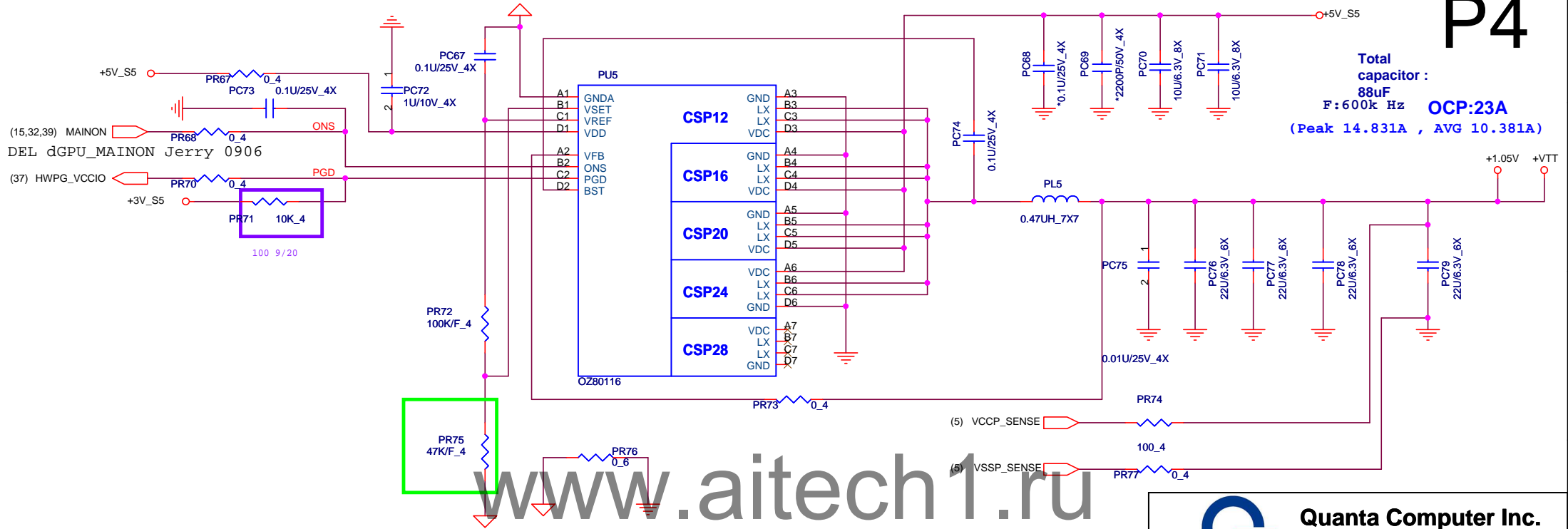
Size	Document Number	Rev
	CUT BAT Control/HOLE	1A
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P4

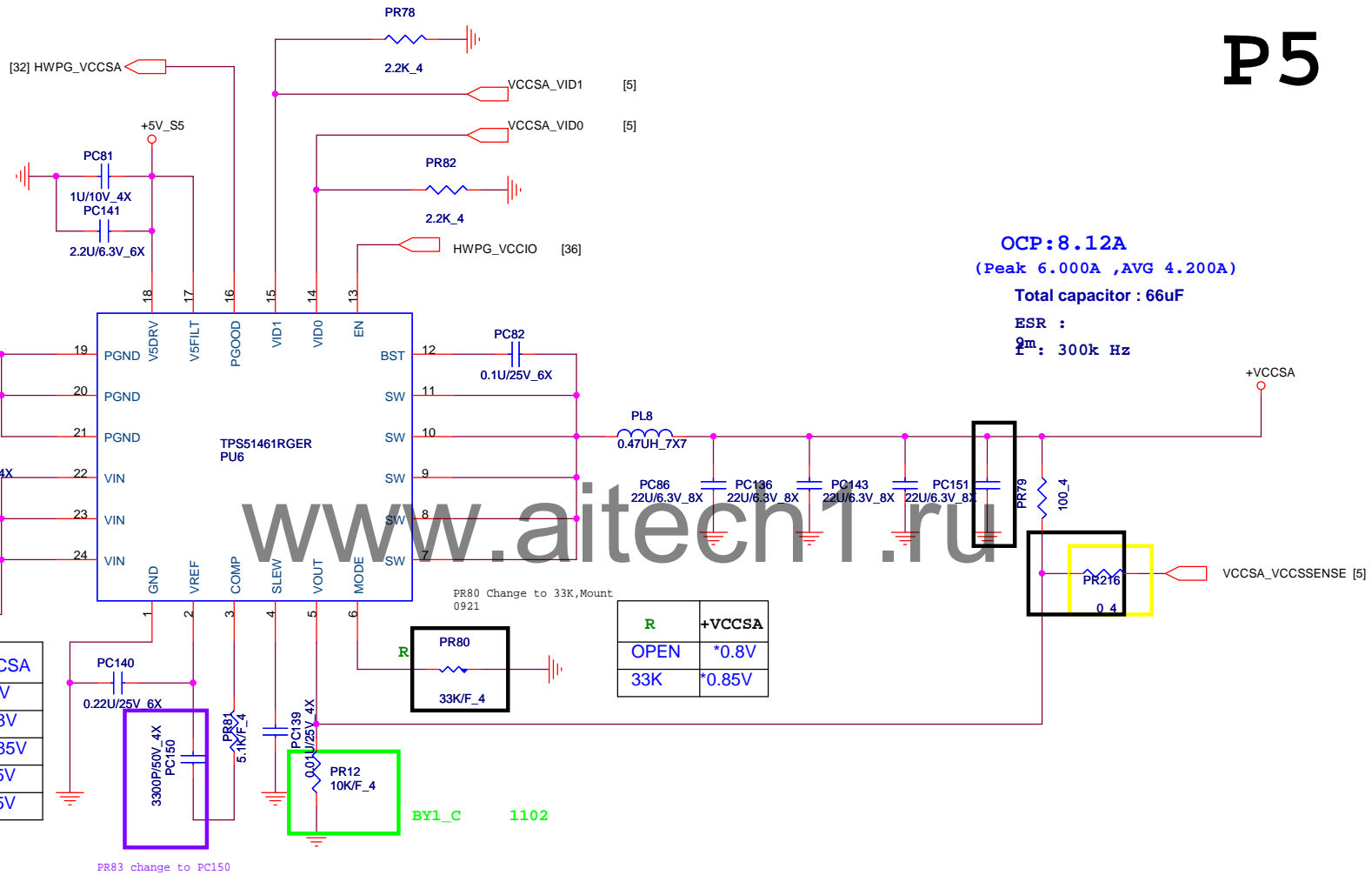


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	VTT/1.05V(OZ80116)	1A
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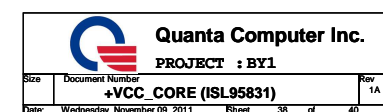
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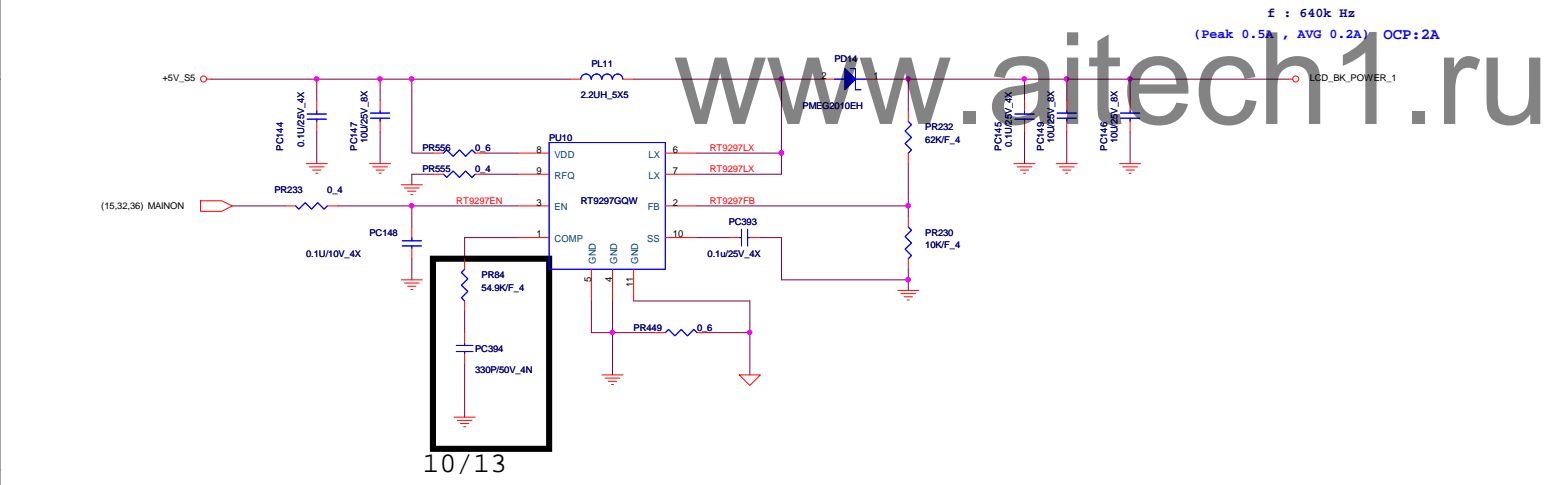
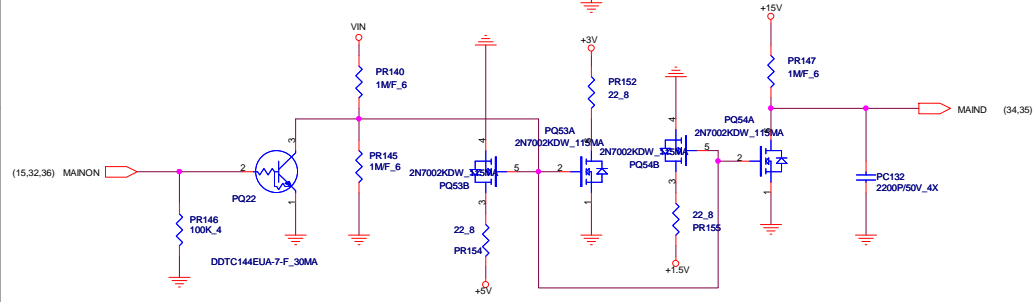
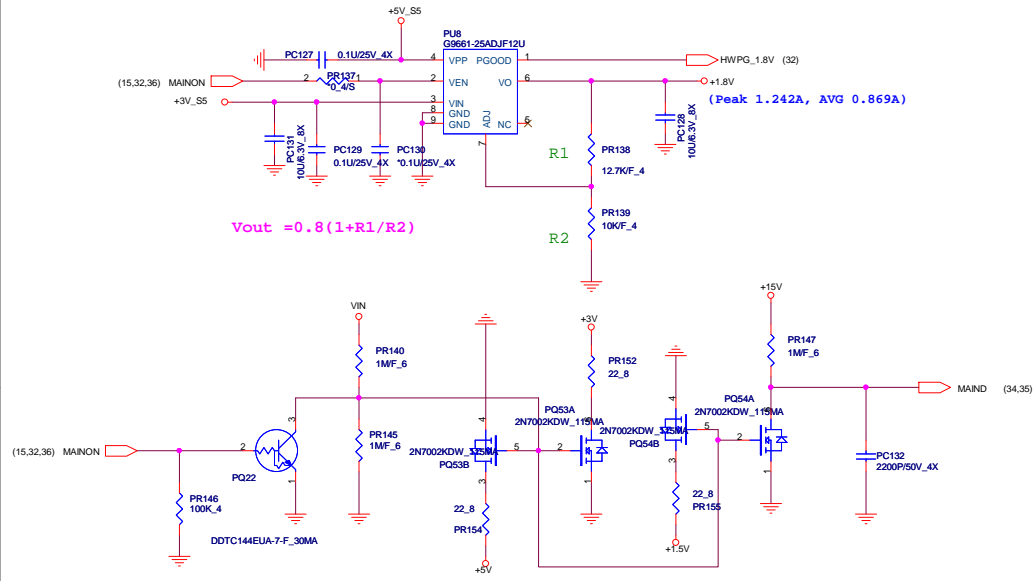


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PROJECT : Chief River

Note 2:
PR205=2.37K: set Vboot=0V & IFL=33A
PR205=294K: set Vboot=1.1V & IFL=33A





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BY1 MB

PAGE 31: HOLE 12 change footprint to h-091x114d91x114n for DXF
PAGE 25: BY1_B Del second hall sensor MR1,R300,C335 for Save space
PAGE 26: Change CN5 P/N to DFHD52MR047 for DXF
PAGE 27: Add R258,R253,R238,R214,R205 for colay with 14600
PAGE 10: Unmount R22,Mount R151 for BIOS Board ID request
PAGE 30: Change R335 from 150 to 1.5k
PAGE 32: BY1_B Add USB_BUS_SW4 -1007
PAGE 32: BY1_B Add LAN_P -1007
PAGE 32: BY1_B Add USB_BUS_SW4 -1007
PAGE 32: BY1_B Add R272
PAGE 32: BY1_B Add USB3_ON -1007
PAGE 32: BY1_B DEL AG_PRESENT -1007
PAGE 31: BY1_B HOLE 12 change footprint to h-091x114d91x114n
PAGE 31: BY1_B HOLE 15,HOLE19,HOLE16 to ground for EMI -1007
PAGE 30: BY1_B Change R335 from 150 to 1.5K
PAGE 30: BY1_B Add L8,L18 with DC09004A014 for EMI -1007
PAGE 30: BY1_B Add CAP for EMI -1007
PAGE 30: BY1_B Add CAP for EMI -1010
PAGE 29: BY1_B Add LAN power control circuit -1007
PAGE 29: BY1_B Del R448 -1007
PAGE 29: BY1_B Add R72 and remove R67 -1007
PAGE 28: BY1_B Mount C199,C224,C379 with 0ohm for EMI -1007
PAGE 27: BY1_B Change for colay with 14600 -1007
PAGE 27: BY1_B Del R183,R184,R129,R130 for Saving spacing 1007
PAGE 25: BY1_B Del second hall sensor MR1,R300,C335 for save space -1006
PAGE 25: BY1_B Mount R359 but Unmount R345
PAGE 25: BY1_B Del F1 1007
PAGE 25: BY1_B Unmount C23 1007
PAGE 25: BY1_B EMI Request 1010
PAGE 11: BY1_B Del R36,R79, R86,R380,R137,L17,R349,R350,R85,R354,R2,R126,L20,C319,R74,R76,R146,L26,C374,R147,R110,R64,R88,R72,R75,R80,R384,R24,R25,R73,C89,R103,R29,R316,C306,C314 for saving spacing-1007
PAGE 11: BY1_B Change for BIOS Board ID request
PAGE 8: BY1_B Change for PCH Dual SPI
PAGE 8: BY1_B Del for saving spacing-1007
PAGE 7: BY1_B Del net AC_PRESENT -1007
PAGE 5: BY1_B Del R198,C174,C179, R124,C151,C393,C394,C400,C401 for saving spacing-1007
PAGE 31: BY1_B Change HOLE1,HOLE4,HOLE7,HOLE8,HOLE9,HOLE10,HOLE11,HOLE18 Footprint 1011
PAGE 7: BY1_B Add C151 For HDMI issue -1011
PAGE 3: BY1_B Change R357 from 24.9k to 25.5k -1013
PAGE 35: BY1_B Unmount PR64_Mount PR83

PAGE 31: BY1_C Del HOLE10 1026
PAGE 30: BY1_C Add R277 for USB issue -1101
PAGE 28: BY1_C C420 Change to 0603 1101
PAGE 27: BY1_C Change L45,L44,L43,L42 P/N
PAGE 27: BY1_C Add R274 for USB Issue 1101
PAGE 25: BY1_C Change to 0805

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MODEL		
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